ABSTRACT OF THE DISCLOSURE

A microprocessor configured to store victimized instruction and data bytes is disclosed. In one embodiment, the microprocessor includes a predecode unit, and instruction cache, a data cache, and a level two cache. The predecode unit receives instruction bytes and generates corresponding predecode information that is stored in the instruction cache with the instruction bytes. The data cache receives and stores data bytes. The level two cache is configured to receive and store victimized instruction bytes from the instruction cache along with parity information and predecode information, and victimized data bytes from the data cache along with error correction code bits. Indicator bits may be stored on a cache line basis to indicate the type of data is stored therein.